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1 Design verification and simulation: Improved symbolic simulation by functional-space decomposition
Tao Feng, Li-C. Wang, Kwang-Ting Cheng
January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair 2004**
Full text available: pdf(195.34 KB) Additional Information: full citation, abstract, references

This paper presents a functional-space decomposition approach to enhance the capability of symbolic simulation. In our symbolic simulator, the control part and data path of a circuit is separated, and their simulated results are recorded in different domains. A 2-tuple list structure is used to separate the results in the control and datapath domains. Then, the functional sub-space in the control domain can further be decomposed in order to achieve the optimal OBDD size and run time. We demonstr ...

2 Cyclic and non-cyclic combinational circuit synthesis: A new enhanced constructive decomposition and mapping algorithm
Alan Mishchenko, Xinning Wang, Timothy Kam
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(241.87 KB) Additional Information: full citation, abstract, references, citings, index terms

Structuring and mapping of a Boolean function is an important problem in the design of complex integrated circuits. Library-aware constructive decomposition offers a solution to this problem. This paper proposes novel techniques to improve the quality and runtime of constructive decomposition. The improvements are effective both in the stand-alone mapping procedure and in the context of re-synthesis applied to a mapped multi-level network. Experiments with public and proprietary benchmarks show ...

Keywords: functional decomposition, re-synthesis, technology mapping

3 Novel self-test methods: A scalable software-based self-test methodology for programmable processors
Li Chen, Srivaths Ravi, Anand Raghunathan, Sujit Dey
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(107.71 KB) Additional Information: full citation, abstract, references, index terms

Software-based self-test (SBST) is an emerging approach to address the challenges of high-

quality, at-speed test for complex programmable processors and systems-on chips (SoCs) that contain them. While early work on SBST has proposed several promising ideas, many challenges remain in applying SBST to realistic embedded processors. We propose a systematic scalable methodology for SBST that automates several key steps. The proposed methodology consists of (i) identifying test program templates tha ...

Keywords: at-speed test, manufacturing test, microprocessor, scalability, software-based self-test, test program

4 CAD: Design topology aware physical metrics for placement analysis

Shyam Ramji, Nagu R. Dhanwada

April 2003 **Proceedings of the 13th ACM Great Lakes symposium on VLSI**

Full text available: pdf(240.08 KB) Additional Information: full citation, abstract, references, index terms

Traditionally placement evaluation metrics have been based on wirelength and congestion measures and are independent of the logic network topology. However, the actual timing measure, which is used in a design closure loop, is path-based and dependent on the network topology. In this paper, we propose a design-topology aware metric that encapsulates the structural property of the circuit and physical goodness of the given placement. We present such a metric which is based on path monotonicity an ...

Keywords: path-monotonicity, placement, timing analysis, wirelength

5 Session 3: From the Trenches (invited): The scaling challenge: can correct-by-construction design help?

Prashant Saxena, Noel Menezes, Pasquale Cocchini, Desmond A. Kirkpatrick

April 2003 **Proceedings of the 2003 international symposium on Physical design**

Full text available: pdf(294.86 KB) Additional Information: full citation, abstract, references, citings, index terms

We present the results of scaling studies in the context of typical block-level wiring distributions, and study the impact of the identified trends on the post-RTL design process. In particular, we look at the implications of exponentially increasing repeater and clocked repeater counts on the algorithms and methodologies used for logic synthesis, technology mapping, layout, and full-chip assembly, and identify several new research problems relevant to future designs. Next, we introduce the basi ...

Keywords: clocked repeaters, correct-by-construction design, design fabrics, interconnect, logic synthesis, placement, post-RTL design, repeaters, routing, scaling, technology mapping

6 Fast seed computation for reseeding shift register in test pattern compression

Nahmsuk Oh, Rohit Kapur, T. W. Williams

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(288.33 KB) Additional Information: full citation, abstract, references, index terms

Solving a system of linear equations has been widely used to compute seeds for LFSR reseeding to compress test patterns. However, as chip size is growing, solving linear equations requires a large number of computations that is proportional to n^3. This paper proposes a new scan chain architecture and algorithm so that the order of computation is proportional to the number of scan cells in a chip. The new architecture is a methodology change that does not require complex Design- ...

7 Poster Session 4: Retiming-based logic synthesis for low-power
Yu-Lung Hsu, Sying-Jyan Wang
August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design**
Full text available: pdf(189.26 KB) Additional Information: full citation, abstract, references, index terms

Power management has become a great concern in VLSI design in recent years. In this paper, we consider the logic level design technique for low power applications. We present a retiming-based optimization method, in which part of the circuit is selected and moved so that it produces logic signals one clock cycle before they are actually applied. If these values can solely determine the output logic level, then the other part of the circuit can be turned-off to save power. We explore acceptable r ...

Keywords: logic design, low-power, retiming, switching actvity

8 Equivalence verification: Automated equivalence checking of switch level circuits
Simon Jolly, Atanas Parashkevov, Tim McDougall
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(220.14 KB) Additional Information: full citation, abstract, references, index terms

A chip that is required to meet strict operating criteria in terms of speed, power, or area is commonly custom designed at the switch level. Traditional techniques for verifying these designs, based on simulation, are expensive in terms of resources and cannot completely guarantee correct operation. Formal verification methods, on the other hand, provide for a complete proof of correctness, and require less effort to setup. This paper presents Motorola's Switch Level Verification (SLV) tool, whi ...

Keywords: MOS circuits, VLSI design, custom design, equivalence checking, formal verification, switch level analysis

9 Automated Modeling of Custom Digital Circuits for Test
S. Bose
March 2002 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(156.90 KB) Publisher Site Additional Information: full citation, abstract

Models meant for logic verification and simulation areoften used for ATPG. For custom digital circuits, these modelscontain many tristate devices, which leads to lower faultcoverage. Unlike other research in the literature, the modelingalgorithms presented in this paper analyze each channelconnected component in the context of its environment,thereby capturing the relationship among its input signals.This reduces the number of tristates and increases the modelingefficiency, as measured by fault ...

10 Congestion-Aware Logic Synthesis
D. Pandini, L. Pileggi, A. Strojwas
March 2002 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(181.11 KB) Publisher Site Additional Information: full citation, abstract

In this era of Deep Sub-Micron (DSM) technologies, the impact ofinterconnects is becoming increasingly important as it relates tointegrated circuit (IC) functionality and performance. In thetraditional top-down IC design flow, interconnect effects are firsttaken into account during logic synthesis by way of wireloadmodels. However, for technologies of 0.25µm and below, thewiring capacitance dominates the gate capacitance and the delayestimation based

on fanout and design legacy statistics can be ...

11 Design for Verification at the Register Transfer Level
Indradeep Ghosh, Krishna Sekar, Vamsi Boppana
January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**
Full text available: pdf(235.31 KB) Publisher Site
Additional Information: full citation, abstract

In this paper we introduce a novel concept that can be used for augmenting simulation based verification at the Register Transfer Level (RTL). In this technique the designer of an RTL circuit introduces some well understood extra behavior (through some extra circuitry) into the circuit under verification. This can be termed as design for verification. During RTL simulation this extra behavior is utilized in conjunction with the original behavior to exercise the design more thoroughly thus making ...

12 An algorithm for bi-decomposition of logic functions
Alan Mishchenko, Bernd Steinbach, Marek Perkowski
June 2001 **Proceedings of the 38th conference on Design automation**
Full text available: pdf(250.63 KB)
Additional Information: full citation, abstract, references, citings, index terms

We propose a new BDD-based method for decomposition of multi-output incompletely specified logic functions into netlists of two-input logic gates. The algorithm uses the internal don't-cares during the decomposition to produce compact well-balanced netlists with short delay. The resulting netlists are provably non-redundant and facilitate test pattern generation. Experimental results over MCNC benchmarks show that our approach outperforms SIS and other BDD-based decomposition methods in ter ...

13 Dynamic detection and removal of inactive clauses in SAT with application in image computation
Aarti Gupta, Anubhav Gupta, Zijiang Yang, Pranav Ashar
June 2001 **Proceedings of the 38th conference on Design automation**
Full text available: pdf(191.57 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we present a new technique for the efficient dynamic detection and removal of inactive clauses, i.e. clauses that do not affect the solutions of interest of a Boolean Satisfiability (SAT) problem. The algorithm is based on the extraction of gate connectivity information during generation of the Boolean formula from the circuit, and its use in the inner loop of a branch-and-bound SAT algorithm. The motivation for this optimization is to exploit the circuit str ...

14 Addressing verification bottlenecks of fully synthesized processor cores using equivalence checkers
G. Subash Chandar, S. Vaideeswaran
January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**
Full text available: pdf(72.23 KB) Additional Information: full citation, abstract, references, index terms

Formal verification plays an important role in the verification of complex processors. In this paper, we discuss the usage and impact of equivalence checking in the verification of TI's TMS320C27X DSP core. During various phases of the design, we need to ensure the correctness of the design, a significant part of which could be best done with an equivalence checker. (For example, verifying the functionality of the netlist after CTS insertion with the one before CTS insertion). The capabilit ...

15 Symbolic functional and timing verification of transistor-level circuits
Clayton B. McDonald, Randal E. Bryant
November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(101.06 KB) Additional Information: full citation, abstract, references, citings, index terms

We introduce a new method of verifying the timing of custom CMOS circuits. Due to the exponential number of patterns required, traditional simulation methods are unable to exhaustively verify a medium-sized modern logic block. Static analysis can handle much larger circuits but is not robust with respect to variations from standard circuit structures. Our approach applies symbolic simulation to analyze a circuit over all input combinations without these limitations. We present a prototype s ...

16 Using partitioning to help convergence in the standard-cell design automation methodology
Hema Kapadia, Mark Horowitz
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(819.81 KB) Additional Information: full citation, references, citings, index terms

17 Enhanced visibility and performance in functional verification by reconstruction
Joshua Marantz
May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**
Full text available: pdf(174.85 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Cycle simulators, in-circuit emulators, and hardware accelerators have made it possible to rapidly model the functionality of large digital designs. But these techniques provide limited visibility of internal design nodes, making debugging hard. Simulators run slowly when all nodes are traced. Emulators provide full visibility only with limited depth, or with greatly reduced speed. This paper discusses software techniques for increasing design visibility while reducing tracing overhead in s ...

Keywords: emulation, functional simulation, reconstruction, visibility

18 Partitioning algorithm to enhance VLSI testability
Bassam Shaer, Sami A. Al-Arian, David Landis
April 1998 **Proceedings of the 36th annual Southeast regional conference**
Full text available: pdf(924.87 KB) Additional Information: full citation, references, index terms

19 Technology mapping for minimizing gate and routing area
Aiguo Lu, Guenter Stenz, Frank M. Johannes
February 1998 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(87.55 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

This paper presents a technology mapping approach for the standard cell technology, which takes into account both gate area and routing area so as to minimize the total chip area after layout. The routing area is estimated using two parameters available at the mapping stage; one is the fanout count of a gate, and the other is the "overlap of fanin level

intervals". To estimate the routing area in terms of accurate fanout counts, an algorithm is proposed which solves the problem of dynamic fanout ...

Keywords: Technology Mapping, Routing, Area Optimization

20 Decomposition methods for library binding of speed-independent asynchronous designs

Polly Siegel, Giovanni De Micheli

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(854.51 KB) Additional Information: full citation, abstract, references, citings, index terms

We describe methods for decomposing gates within a speed-independent asynchronous design. The decomposition step is an essential part of the library binding process, and is used both to increase the granularity of the design for higher quality mapping and to ensure that the design can be implemented. We present algorithms for simple hazard-free gate decomposition, and show results which indicate that we can decompose most of the gates in our benchmark set by this simple method. We then exte ...

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